MULTIPLEXING PRISM CMOS IMAGERS TO A SINGLE DATA BUS

This application claims priority to U.S. Provisional Application serial number 60/450,086 filed on February 26, 2003, and herein incorporated by reference.

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to solid state optical imagers, and, more particularly, to a method to address a reconfigurable array of imagers using a single fixed size data bus.

(2) Description of the Prior Art

Solid state imagers are used in many applications. Typically, these imagers comprise fixed arrays of pixels. It is difficult to reconfigure these imagers into large arrays or into higher resolution arrays. This is especially true when attempting to create high-resolution arrays using fixed data bus architecture.

Several prior art inventions relate to optical imaging using CMOS image devices. U.S. Patent 6,176,429 B1 to Redderson et al describes an optical reader using a photosensor that may comprise a multidimensional CMOS array. U.S. Patent 6,505,003 B1 to Malloy Desormeaux discloses a hybrid camera using a CMOS image sensor.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method and device to access an array of imagers.

A further object of the present invention is to provide a method whereby a plurality of imagers can be used cooperatively to improve image resolution or to provide a single, large resolution image.

A yet further object of the present invention is to provide a means to reconfigure an n x m array of imagers using a single data bus architecture.

In accordance with the objects of this invention, a method of addressing imagers is achieved. The method comprises, first,

providing a bi-directional bus. An array of imagers is arranged in n rows and m columns wherein the n and m are positive integers. Each imager is connected to the bi-directional bus. Each imager has a Vmode terminal. Each imager has a select terminal. Each imager can deliver a signal to the bi-directional bus only when a first selecting signal is applied to a Vmode terminal of that imager and a second selecting signal is applied to a select terminal of that imager simultaneously. A first multiplexer has a vertical select input and n outputs. Each of the n outputs is connected to one of the Vmode terminals of the imagers. A second multiplexer has a horizontal select input and n x m outputs. Each output is connected to the select terminal of one of the imagers. A vertical input signal is applied to the vertical select input of the first multiplexer thereby producing the first selecting signal at one of the Vmode output lines. A horizontal input signal is applied to the horizontal select input of the second multiplexer thereby sequentially producing the second selecting signal at the select terminal of one of the imagers.

Also in accordance with the objects of this invention, a method of accessing an imager array is achieved. The method comprises, first, providing a bi-directional bus. An array of imagers is arranged in n rows and m columns. The n and m are

positive integers. Each imager is connected to the bi-directional bus. A line of bits of any imager is accessible by a line address. A column counter, a row counter, and the line address are initialized to zero. All of the array is accessed. The accessing comprises further steps of, first, accessing one line of one the imager corresponding to the line address, the column counter, and the row counter. Thereafter the column counter is tested for equality to m-1. If not equal, the column counter is incremented and the step of accessing one line is repeated. If equal, the column counter is reset. Thereafter the line address is tested for equality to total lines in each imager. If not equal, the line address is incremented and the step of accessing one line is repeated. If equal, the line address is reset. Thereafter the row counter is tested for equality to n-1. If not equal, the row counter is incremented and the step of accessing one line is repeated. If equal, the step of accessing all is completed.

Also in accordance with the objects of this invention, a multiple imager array device is achieved. The device comprises, first, a bi-directional bus. An array of imagers is arranged in n rows and m columns. The n and m are positive integers. Each imager is connected to the bi-directional bus. A line of bits of any imager is accessible by a line address. Each imager has a

Vmode input and an output enable input. The Vmode input and the output enable input must be enabled to allow accessing. A first multiplexer has an input and a plurality of outputs. The input is connected to a column counter. Each output is connected to the output enable input of one of the imagers. A second multiplexer has an input and a plurality of outputs. The input is connected to a row counter. Each output is connected to the Vmode input of each imager in one of the rows.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Fig. 1 illustrates a first preferred embodiment of the present invention showing a 2 x 3 array of imagers connected to a single, bi-directional bus.

Fig. 2 illustrates a block diagram of a single imager.

Fig. 3 illustrates a second preferred embodiment of the present invention showing how the column count and the row count are generated from the horizontal clock and the line address,

respectively and showing how the select signals (SEL1:SEL(mxn)) are generated from the sum of the column count and row count signals.

Fig. 4 illustrates a third preferred embodiment of the present invention showing a method to access an imager array having a single, bi-directional bus.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the present invention disclose a method and a device for accessing an imager array having a single, bi-directional bus. It should be clear to those experienced in the art that the present invention can be applied and extended without deviating from the scope of the present invention.

Referring now to Fig. 1, the first preferred embodiment of the present invention is illustrated. Several important features of the present invention are shown and discussed below. This invention relates to an n x m array of imagers connected to a single bi-directional bus. As an example, a 2 x 3 array of six imagers 101, 102, 103, 210, 202, and 203 with each of the

imagers connected to a single bi-directional bus 100 is shown in Fig. 1. An example of a single imager 20 is shown in Fig. 2. This imager has an output port 24 for connection to the bus. In this imager 20 a signal at the Vmode terminal 22 controls whether or not the imager 20 is connected to the bus. A select terminal 26 selects a particular imager 20. An address bus ADDRESS 28 is used to select which row or line of bits is accessed. For the imager to deliver a signal to the bus both the Vmode terminal 20 and the select terminal 26 must be activated.

Returning again to Fig. 1, the six imagers are arranged in an array of two rows of three imagers in each row. Imagers 101, 102, and 103 are in the first row and have output ports 110, 112, and 114 connected to the bi-directional bus 100. Imagers 201, 202, and 203 are in the second row and have output ports 210, 212, and 214 connected to the bi-directional bus 100. A vertical select line 306 is connected to a first multiplexer 300. The first multiplexer 300 has a Vmode output line for each row of imagers.

In this example, there are two rows of imagers and the first multiplexer 300 has a first Vmode line 302 and a second Vmode line 304. The first Vmode line 302 is connected to the Vmode terminals 104, 106, and 108 of the imagers 101, 102, and

103 in the first row. The second Vmode line 304 is connected to the Vmode terminals 204, 206, and 208 of the imagers 201, 202, and 203 in the first row. If there were more imagers in each row of the array, the Vmode terminals of all the imagers in the first row would be connected to the first Vmode line, and the Vmode terminals of all the imagers in the second row would be connected to the second Vmode line. If there were additional rows of imagers, then the first multiplexer 300 would have a Vmode line for each row of imagers in the array. The input to the first multiplexer 300 is a vertical select line 306.

A horizontal select line, COLUMN COUNT, 402 is connected to a second multiplexer 400 which has an output line for each imager in the array. One of the output lines of the second multiplexer 400 is connected to the select terminal 116, 118, 120, 216, 218, and 220 of each imager 101, 102, 103, 201, 202, and 202 in the array. With this arrangement, the vertical select line, ROW COUNT, 306 causes the multiplexer to activate either the first Vmode line 302 or the second Vmode line 304. The horizontal select line then causes the second multiplexer 400 to activate the select terminal of a particular imager so that the signal from that imager is sent to the bi-directional bus 100.

In an n x m array of imagers, the vertical address selects the n imagers in row m. The input to the second multiplexer 400 then causes an output of the second multiplexer 400 to enable the output port of a single imager to be active and the signal of that imager to be transferred to the bi-directional bus 100. By using the vertical select address as the write enable pulse, an entire row is selected and transferred to n horizontal registers. This line is read out serially.

This method provides a means to reconfigure the array of imagers n x m without bounds while maintaining the same data bus architecture. This application could be implemented with slightly overlapping optics to provide a seamless combining of imager data to provide a single, large resolution image. This has application in fixed object plane imaging which includes X-ray imagers and facsimile. Also, several remote sources could be multiplexed onto a single display for security applications.

Referring again to Fig. 1, the first preferred embodiment of the present invention may be further described. The device comprises, first, a bi-directional bus 100. An array of imagers I1-I6 101, 102, 103, 201, 202, and 203 is arranged in n rows and m columns. In this case, n = 2 rows and m = 3 columns. Each imager is connected 110, 112, 114, 210, 212, and 214 to the bi-

directional bus 100. A line of bits of any imager is accessible by a line address LINE ADDRESS 407. Each imager 101, 102, 103, 201, 202, and 203 has a Vmode input and an output enable input. The Vmode input and the output enable input must be enabled to allow accessing. A first multiplexer MUX2 400 has an input 402 and a plurality of outputs SEL1-SEL6 116, 118, 120, 216, 218, and 220. The input is connected to a column counter COLUMN COUNT 402. Each output SEL1-SEL6 is connected to the output enable input of one of the imagers I1-I6. A second multiplexer MUX1 300 has an input 306 and a plurality of outputs 302 and 304. The input is connected to a row counter ROW COUNT 306. Each output VMODE1 302 and VMODE2 304 is connected to the Vmode input of each imager in one of the rows.

Referring now to Fig. 3, a second preferred embodiment of the present invention is illustrated. This embodiment shows how the column counter COLUMN COUNT 402 and the row counter ROW COUNT 306 are preferably generated. The horizontal clock HCLK 435 comprises a synchronous clock used to clock data into or out from the imager devices in the array. In the preferred embodiment example, the HCLK 435 comprises a 36 MHz signal. A first divider 420 is used to divide the HCLK 435 by the number of horizontal bits per line in each imager. For example, if the imagers are each 640 bits/line x 480 lines, then the HCLK 435 is

divided by 640 to create the signal COLUMN COUNT 402. The COLUMN COUNT 402 is a multiple bit signal that effectively counts each time an imager is read by the HCLK signal. In the preferred embodiment, the bi-directional bus clocks data into or out from the imager in serial fashion. If the imager has 640 horizontal bits per line, then it requires 640 clock cycles to clock in or out the data bits for that single line in that single imager. Therefore, during clock cycles 0 through 639, the COLUMN COUNT = 0, during clock cycles 640 through 1279, the COLUMN COUNT = 1, and during clock cycles 1280 through 1919, the COLUMN COUNT = 2. To count from 0 to 2, COLUMN COUNT would therefore have to be two bits wide. Moreover, during COLUMN COUNT = 0, the first column of imagers is accessed, during COLUMN COUNT = 1, the second column of imagers is accessed, and during COLUMN COUNT = 2, the third column of imagers is accessed.

The LINE ADDRESS signal 407 comprises the address bus used to select which row of any imager is read/written. The LINE ADDRESS signal 407 is divided by the number of lines (rows) in each imager. In the preferred case, this means that the LINE ADDRESS signal is divided by 480 to create the ROW COUNT 306. Therefore, the LINE ADDRESS between 0 and 479 reads the top row of imagers, the LINE ADDRESS between 480 and 959 reads the

bottom row of imagers. Since there are only two rows of imagers in the preferred embodiment, the ROW COUNT 306 is only 0 or 1 and can be carried by a single line.

In this preferred embodiment, the COLUMN COUNT 402 and the ROW COUNT 306 are both input into the first multiplexer MUX2 400. The combined sum can be written COLUMN COUNT:ROW COUNT as a bus input to the MUX2 400. The outputs of the first multiplexer MUX2 400 are the selection signals SEL1 to SEL(mxn) in the general case. The ROW COUNT signal is used by the second multiplexer MUX1 300 to generate the Vmode signals VMODE1 to VMODEn in the general case.

It is found that this approach can provide a means to extend the m x n array of imagers, without bounds, while maintaining the same data bus architecture. For example, using the m = 3 array, the maximum frame rate would be 30/m Hz. Therefore, a 3 x 2 array with a minimal overlap would provide a 2076 x 1008 resolution at 15 frames/second. Further, this application could be implemented with slightly overlapping optics to provide seamless combining of imager data and to provide a single, large resolution image. This has application in fixed object plane imaging which may include X-ray imagers

and facsimile. Also, several remote sources could be multiplexed onto a single display for security applications.

Referring now to Fig. 4, a third preferred embodiment of the present invention is illustrated. The method 500 of accessing (read/write) imager data in an imager array is shown. The method comprises initializing the column counter, the row counter, and the line address to zero in step 510. One line of one the imager is accessed corresponding to the line address, the column counter, and the row counter in step 515. Thereafter the column counter is tested for equality to m-1 in step 520. If not equal, the column counter is incremented and the step of accessing one line is repeated in step 525. If equal, the column counter is reset in step 530. Thereafter the line address is tested for equality to total lines in each imager in step 535. If not equal, the line address is incremented and the step of accessing one line is repeated in step 540. If equal, the line address is reset in step 545. Thereafter the row counter is tested for equality to n-1 in step 550. If not equal, the row counter is incremented and the step of accessing one line is repeated in step 555. If equal, the step of accessing all is completed.

The advantages of the present invention may now be summarized. An effective and very manufacturable method and device to access an array of imagers is achieved. A method whereby a plurality of imagers can be used cooperatively to improve image resolution or to provide a single, large resolution image is achieved. A means to reconfigure an n x m array of imagers using a single data bus architecture is provided.

As shown in the preferred embodiments, the novel method and device of the present invention provides an effective and manufacturable alternative to the prior art.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is: